RECEIVE AND TRANSMIT BLOCKS FOR ASYNCHRONOUS TRANSFER MODE (ATM) CELL DELINEATION

TECHNICAL FIELD OF THE INVENTION

This invention relates in general to asynchronous transfer mode (ATM) communication and, more particularly, to receive and transmit blocks for asynchronous transfer mode (ATM) cell delineation.

BACKGROUND OF THE INVENTION

Asynchronous transfer mode (ATM) communication systems are widely used for network communications. In general, ATM communication protocols involve stacks having several layers including a physical layer as the lowest layer. The ATM physical layer typically involves the movement of cells between source and target physical layer devices. The cells are often moved across a bus in smaller parallel sets of data. When the data reaches the target device, the cell is reconstructed and then sent up the stack to its final destination. One example of an ATM physical layer protocol is the Utopia 2 protocol. In implementing a physical layer bus, one problem that arises is cell delineation and the transfer of cells across the physical bus.

SUMMARY OF THE INVENTION

In accordance with the present invention, receive and transmit blocks for asynchronous transfer mode (ATM) cell delineation are disclosed that provide advantages over conventional cell delineation schemes.

According to one aspect of the present invention, a receive block for asynchronous transfer mode (ATM) cell delineation has a plurality of cell delineation blocks. Each cell delineation block is coupled to receive an associated serial bit stream, and each cell delineation block operates to identify ATM cell boundaries in the serial bit stream and to convert ATM cell payloads to parallel data words. The receive block also has a memory which has a plurality of memory blocks organized with each memory block associated with a cell delineation block. Each of the memory blocks has a plurality of ATM cell storage locations. A memory controller is coupled to the cell delineation blocks and the memory. The memory controller operates to read data words from the cell delineation blocks and to write data words to one of the cell storage locations in associated memory blocks. A bus controller is coupled to the memory controller and to the memory. The bus controller operates to interface with an ATM physical layer, to receive a memory status signal from the memory controller and to provide signals to the memory for communicating an ATM cell across the ATM physical layer. According to one implementation, the bus controller further receives address mode/select signals and operates to respond to one of a plurality of subsets of port addresses on the ATM physical layer responsive to the address mode/select signals.

According to another aspect of the present invention, a transmit block for asynchronous transfer mode (ATM) cell delineation has a bus controller that operates to interface with an ATM physical layer. The

bus controller receives ATM cells across the ATM physical layer and converts ATM cell payloads to output parallel data words. The transmit block further has a plurality of queue memories that each have a plurality of cell storage locations. A plurality of queue select devices are coupled to the bus controller and receive the output parallel data words. Each queue select device provides the output parallel data words to one of the plurality of cell storage locations in an associated queue memory. A plurality of cell delineation blocks each receive parallel data words from an associated queue memory. Each cell delineation block operates to convert parallel data words to a serial bit stream carrying ATM cell payloads. According to one implementation, the bus controller further receives address mode/select signals and operates to respond to one of a plurality of subsets of port addresses on the ATM physical layer responsive to the address mode/select signals.

A technical advantage of the present invention is the use of a memory controller in the receive block which interfaces between cell delineation blocks and memory such that one block of memory can service all receive cell delineation blocks.

Another technical advantage is the use of a bus controller that can respond to different port addresses based upon input settings. This allows the same bus controller design to be used for different ports on the same physical layer bus. Further, the reduction in the number of ports reduces the load seen by the physical layer bus.

Other technical advantages should be readily apparent to one of ordinary skill in view of the description, drawings and claims.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete understanding of the present invention and advantages thereof may be acquired by referring to the following description taken in conjunction with the accompanying drawings, in which like reference numbers indicate like features, and wherein:

FIGURE 1 is a block diagram of one embodiment of a portion of a network interface module in an XDSL communication system;

FIGURE 2 is a block diagram of one embodiment of a receive block within the system of FIGURE 1;

FIGURE 3 is a block diagram of one embodiment of the organization of the memory in the receive block of FIGURE 2;

FIGURE 4 is a block diagram of one embodiment of a cell delineation block of FIGURE 2;

FIGURE 5 is a block diagram of one embodiment of a transmit block within the system of FIGURE 1; and

FIGURE 6 is a block diagram of one embodiment of a cell delineation block of FIGURE 5.

DETAILED DESCRIPTION OF THE INVENTION

FIGURE 1 is a block diagram of one embodiment of a portion of a network interface module in an XDSL communication system. As shown, the system includes an asynchronous transfer mode (ATM) switch 10 that has a physical layer interface to cell delineation transceivers 12. ATM switch 10 and cell delineation transceivers 12 communicate ATM cells on the physical layer interface. In the illustrated embodiment, the physical layer interface is a Utopia 2 interface. Cell delineation transceivers 12 are connected to a plurality of ADSL transceiver units 14 located at a central office (ATU-C). U.S. Patent No.5,668,857 provides an example of a communication system in which the system of FIGURE 1 might be used. As shown, cell delineation transceivers 12 comprise a plurality of receive blocks 16 and transmit blocks 18. These blocks are organized in pairs of one receive block 16 and one transmit block 18, and each pair handles a specified set of port addresses on the ATM physical interface. For example, each pair of the receive blocks 16 and transmit blocks 18 handle a subset (e.g., eight addresses) of the 31 port addresses on the Utopia 2 interface.

In operation, a serial bit stream from an ADSL transceiver unit 14 is received by a receive block 16. Receive block 16 then delineates the serial bit stream into ATM cells which are then communicated across the physical interface to ATM switch 10. Conversely, ATM cells from ATM switch 10 are delineated and communicated across the physical interface to one of the transmit blocks 18. That transmit block 18 then converts the ATM cell into a serial bit stream which is provided to the appropriate ADSL transceiver unit 14.

FIGURE 2 is a block diagram of one embodiment of a receive block 16 within the system of FIGURE 1. As

shown, receive block 16 comprises a plurality of cell delineation blocks 20. Each cell delineation block 20 is connected to a memory controller 22 via a 16-bit data word line and provides a word-ready signal. Memory controller 22 is coupled to a bus controller 24 (e.g., Utopia 2 controller) and a memory 26. As shown, memory controller 22 provides a memory status signal to bus controller 24 and provides a write address and a write enable signal to memory 26 in addition to 17 bits of data (one bit of parity data). Bus controller 24 receives address mode/select signals which determine to which bus port addresses bus controller 24 responds. In general, an address on the physical layer interface, such as a Utopia 2 address, directly maps to one of the cell delineation channels. In one implementation, bus controller 24 responds to addresses as follows:

mode select		address	address (w/ arbitration)
1	0		
0	0	7:0	7:1, 17
0	1	15:8	15:9, 16
1	0	23:16	n/a
1	1	30:24	n/a

Further, bus controller 24 receives the physical interface signals (e.g., Utopia 2) as shown: receive address, cell available (clav), enable (enb_), start of cell (soc) and clock. Bus controller 24 also receives an enable_clav signal and an arbitration enabled signal. One arbitration scheme using these signals is disclosed in U.S. Patent Application Serial No. _____, entitled "System and Method of Operation for Managing

Data Communication Between Physical Layer Devices and ATM Layer Devices", the disclosure of which is incorporated herein by reference.

In operation, cell delineation blocks 20 receive serial bit streams from ADSL transceiver units 14. The cell delineation blocks 20 identify cell boundaries and separate cells carried by the bit streams and convert the cells to 16-bit parallel data words. As data words are ready, cell delineation blocks 20 provide word-ready signals to memory controller 22, along with the 16 bits of data. Memory controller 22 polls cell delineation blocks 20 in round-robin fashion. When a read-word signal is found, memory controller 22 reads the data words, and in turn provides a write address and write enable signal to memory 26 along with 17 bits of data (including an added parity bit). When an entire cell has been constructed in memory 26 for one of the cell delineation units 20, memory controller 22 provides a memory status signal to bus controller 24 indicating that a cell is ready to be transferred across the physical layer interface. In this case, bus controller 24 provides a read address on the address lines to memory 26 and signals memory 26 to enable output (oen). Memory 26 then causes the cell data to appear on the output data pins of memory 26. Bus controller 24 also signals the physical layer interface that a cell is available (Rx clav). In general, bus controller 24 responds with the cell available signal in response to seeing its address on the physical layer address lines. However, bus controller 24 does receive an "enable_clav" signal which prevents bus controller 24 from responding with a cell available until it is enabled to do so.

As shown and mentioned above, the address mode/select signals provided to bus controller 24 indicate to which port addresses bus controller 24

responds (7:0, 15:8, 23:16 or 30:24). Thus, using the address mode/select pins, bus controller 24 can be used to control receive block 16, for example, for responding to any of the thirty one ports of a Utopia 2 interface. Further, bus controller 24 has an arbitration mode which can be enabled. In this mode, bus controller 24 does not respond to ports 0 or 8 to allow other devices to respond to those addresses. Further, in this mode, the enable_clav signal can be used to prevent bus controller 24 from responding to an address on the physical interface.

Cell delineation blocks 20 are responsible for receiving serial data from the ADSL transceiver unit and searching for the beginning of ATM cells (cell delineation). When valid cells are being received, cell delineation blocks 20 pass the data words to one of the two receive buffers in memory 26 (see below). When a full cell has been received, that cell is passed across the receive portion of the physical layer (e.g., Utopia 2 bus).

Cell delineation is the process which allows identification of the cell boundaries. The ATM cell begins with a four byte header that is protected with a one byte HEC code that was generated with the polynomial $x^8 + x^2 + x + 1$. The cell delineation algorithm generally follows a state machine with three states: HUNT, PRESYNC and SYNC. In the HUNT state, the delineation process is performed by checking bit by bit for the correct HEC for the assumed header field. This is accomplished in the cell delineation blocks 20, for example, with a forty bit shift register whose input is ARXD and is clocked by ARXC. At every bit time, the HEC is calculated across the last 32 bits of the shift register (4 bytes of header), x55 is added to the calculated HEC and compared to the bits in the first eight bits of the shift

register. If a match is found then the cell delineation state machine goes into the PRESYNC state.

In the PRESYNC state, the cell delineation state machine waits a full cell time (424 clocks) to calculate the HEC across the last 32 bits of the input shift register and compare to the HEC field in the first byte of the shift register. If a match is not found, the state machine goes back into the HUNT state where on every clock the HEC is calculated. If a correct match is found an internal "correct HEC" counter is incremented. The PRESYNC state continues to search for correct HEC at every cell time. When six (DELTA value recommended by ITU-T I.432) cells pass through with correct HEC values, the cell delineation state machine goes into the SYNC state. At this time the RLOF output goes inactive low to indicate that the cell delineation state machine has correctly found the boundary of ATM cells.

In the SYNC state, at every cell time, the cell delineation state machine still checks for the correct HEC. If an incorrect HEC is found an internal "incorrect HEC" counter is incremented. If seven (ALPHA value recommended by ITU-T I.432) consecutive cells are found with the incorrect HEC, the cell delineation state machine reverts back to the HUNT state. The loss of cell delineation is indicated by the activation of the RLOF output. Cells with an incorrect HEC value and IDLE cells are dropped during the SYNC state. Cells with any HEC error are considered to have multiple bit errors. Therefore single bit error correction is not performed on cells who only have a single bit error in the HEC and that cell will be dropped. This operation corresponds to the ADSL Forum's ATM Mode Technical Group working text (WT-006-R7).

Starting in the PRESYNC state where a pseudo ATM cell boundary is determined, the payload data of the ATM

cell will be sent through a self-synchronizing descrambling circuit (see FIGURE 4) that will be responsible for descrambling the incoming scrambled payload bit stream. As soon as 43 bits of payload data are shifted in, the descrambling circuit will be in sync with the transmitting scrambler and the rest of the payload data bits will be descrambled properly. Only during the SYNC state are non-IDLE ATM cells with the correct HEC byte passed to the internal receive memories. During this state, the bit stream passes through a serial to parallel shift register and words of data are written to memory.

FIGURE 3 is a block diagram of one embodiment of the organization of the memory 26 in a receive block 16 of FIGURE 2. As shown, memory 26 is organized into a plurality of blocks 30 each dedicated to one of the cell delineation blocks 20. Each memory block 30 comprises segmented storage space for two cells (cell 0, cell 1) associated with that cell delineation block 20.

In operation, the address bits provided to memory 26 are used to select to which block 30 data is to be written. The selection is determined based upon the source cell delineation block and which cell (0 or 1) is next to be used. For example, address bits 8:6 can be used to select the memory block 30 (based upon the source cell delineation block) and address bits 5:0 can be used to select the location for that memory block 30. The two available cell storage spaces can be used in a ping-pong manner to essentially create a two deep queue for cell data written into a memory block 30 for a particular cell delineation block 20.

FIGURE 4 is a block diagram of one embodiment of a cell delineation block 20 of FIGURE 2. As shown, cell delineation block 20 comprises a cell delineation unit 40, a descrambling circuit 42 and a serial/parallel

converter 44. Cell delineation unit 40 receives signals from an ADSL transceiver unit including a serial clock and serial data. Cell delineation unit 40 also receives a serial loop clock and a serial loop data from an associated transmit cell delineation unit. This loop can be used to test the physical interface without having to couple it with operating ATU-C's. Cell delineation unit 40 provides an output signal that indicates a loss of frame (RLOF) with respect to the serial bit stream from the ADSL transceiver unit.

Cell delineation unit 40 separates the serial bit stream into cells and provides an output of serial data to descrambling circuit 42. Descrambling circuit 42 then descrambles the data and provides a descrambled serial bit stream to serial/parallel converter 44. Serial/parallel converter 44 then converts the serial bit stream to a parallel data words being provided to the memory controller. As shown, a scramble signal is provided to descrambling circuit 42 in case the serial bit stream does not need to be descrambled.

FIGURE 5 is a block diagram of one embodiment of a transmit block 18 within the system of FIGURE 1. As shown, transmit block 18 comprises a bus controller 50. Bus controller 50 is connected to a plurality of queue select devices 52 (1:2 multiplexers) which select between a pair of queue memories 54 associated with each cell delineation block 56. Each cell delineation block 56 is, in turn, connected to an ADSL transceiver unit. Bus controller 50 receives physical layer interface signals including: data, address, enb_, soc and clock signals. Bus controller 50 provides a transmit clav signal to the physical interface. Further, analogous to the above discussion, bus controller 50 receives address mode/select signals that determine to which physical layer addresses bus controller 50 responds. In one

implementation, bus controller 50 responds to addresses as follows:

mode select		address	address (w/ arbitration)
1	0		
0	0	7:0	7:1, 17
0	1	15:8	15:9, 16
1	0	23:16	n/a
1	1	30:24	n/a

In operation, bus controller 50 receives ATM cell data from the physical layer. Bus controller 50 then provides data words to an appropriate queue select device 52 and queue memory 54 depending upon the target ADSL transceiver unit. Queue select device 52 allows a ping-pong selection between queue memories 54 for writing to one of the pair of cell storage spaces associated with the cell delineation block 56. For example, cell 0 is written first and then transferred to cell delineation block 56, and the next cell will be written into cell 1. The cell delineation blocks 56 convert the 16 bit parallel data words to a serial bit stream which is then provided to the ADSL transceiver units.

When one of the transmit queue memories 54 has been written with a full ATM cell, the status of that buffer memory will be transferred to an ADSL transmit state machine. This status bit is synchronized to the ATXC clock since the ADSL transmit state machine is running at a different rate than the transmit state machine. When the ADSL transmit state machine has finished transmitting an IDLE cell or a normal cell, and it detects that one of the buffer queue memories 54 has a new cell to send, then it will read the first byte out of that queue memory 64.

The data will be loaded and will be shipped out the ATXD output on the rising edge of ATXC.

After the first five bytes (the cell header) have been read from the memory and serially sent out the ATXD output, the next 48 bytes (the cell payload) are serially sent out the ATXD output after passing through a data scrambling circuit. The scrambling circuit is enabled if a SCRAMBLE signal is set for the cell delineation block 56. Scrambling should be turned on during normal operation and is generally only turned off for diagnostic purposes. The scrambling circuit can be a self-synchronizing scrambler as described in the ITU-T I.432 specification using the polynomial $x^{43} + 1$. The scrambler randomizes the bits from the payload field and is disabled when the five bytes of the ATM header are being transmitted. This randomization of data improves the performance and security of the cell delineation circuit that will be receiving the data. The scrambler is a 43 bit shift register whose input is driven by the exor of the payload data bit and the last bit of the shift register. ATXD can also be driven from the output of the exor.

When a cell has been completely transmitted, an ADSL transmit state machine sends a signal back to the transmit state machine to indicate that it has emptied one of the transmit buffer memories so that it can be used to store another cell. It also checks the status of the two transmit buffer queue memories 54. If neither of the queue memories 64 has a full cell to be transmitted, an IDLE cell will be sent. An IDLE cell is composed, for example, of the first through fifth bytes being x00, x00, x00, x01, and x52 with the payload being 48 identical bytes of value x6a.

FIGURE 6 is a block diagram of one embodiment of a cell delineation block 56 of FIGURE 5. As shown, cell

delineation block 56 includes a multiplexer 60 which selects between one of the two 16 bit data word inputs from associate queue memories 54. Multiplexer 60 then provides the parallel data word to a parallel/serial converter 62. Parallel/serial converter 62 converts the data word to a serial bit stream which is provided to a scrambling circuit 64. Scrambling circuit 64 receives a clock signal from an associated ADSL transceiver unit and provides a serial bit stream to that ADSL transceiver unit. Scrambling circuit 64 also provides a loop clock and loop data to a receive cell delineation block for testing the physical layer without needing to install it in an operating system. In addition, scrambling circuit 64 receives a scramble signal that indicates whether scrambling needs to be done.

Although the present invention has been described in detail, it should be understood that various changes, substitutions and alterations can be made thereto without departing from the spirit and scope of the invention as defined by the appended claims.